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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,495	12/31/2003	David W. Hartwell	200313714-1	1809

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EXAMINER	
IQBAL, NADEEM	

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,495	HARTWELL ET AL.	
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1, 2, 14, 15, 20-22, & 29 are rejected under 35 U.S.C. 102(e) as being anticipated by Cypher (U.S. Patent application number 2004/0088636).

2. As per claims 1 & 29, Cypher teaches (Page 1, para. 0009, lines 1-4) a memory controller that includes a check/correct circuit and a data remap circuit. He also teaches (Page 1, para. 0009, lines 7-9) that the check/correct circuit is configured to detect a failure of the memory devices. He thus teaches determining a type of the error. He also teaches data remap control circuit is configured to cause a remap of each of a plurality of encoded data blocks to avoid storing bits in the failing memory device. He thus teaches configuring access to the memory module based on the error type.

3. As per claim 2, With reference to enabling access to the failed memory module when the error type is determined to be soft. He teaches (Page 3, para. 0039, lines 7-9). With reference to disabling access to the failed memory module when the error type is determined to be hard. He teaches (Page 3, para. 0039, lines 11-14).

4. As per claims 14 & 15, Cypher teaches (Page 1, para. 0009, lines 1-4) a memory controller that includes a check/correct circuit and a data remap circuit. He also teaches (Page 1, para. 0009, lines 7-9) that the check/correct circuit is configured to detect a failure of the memory devices. He thus teaches a plurality of data storage devices and a memory controller that accesses the data storage devices. He also teaches data remap control circuit is configured to

cause a remap of each of a plurality of encoded data blocks to avoid storing bits in the failing memory device. He thus teaches an error type controller that configures the access such that the memory controller can continue to access a failed one of the plurality of the storage devices that incurred a soft error.

5. As per claim 20, Cypher teaches (Page 1, para. 0009, lines 1-4) a memory controller that includes a check/correct circuit and a data remap circuit. He also teaches (Page 1, para. 0009, lines 7-9) that the check/correct circuit is configured to detect a failure of the memory devices. He thus teaches redundant memory logic and a memory controller that independently controls read and writes access to a failed one of the plurality of data storage devices. With reference to disabling access to the failed memory module when the error type is determined to be hard or soft error. He teaches (Page 3, para. 0039, lines 11-14).

6. As per claims 21 & 22, With reference to enabling access to the failed memory module when the error type is determined to be soft. He teaches (Page 3, para. 0039, lines 7-9). With reference to disabling access to the failed memory module when the error type is determined to be hard. He teaches (Page 3, para. 0039, lines 11-14).

7.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 3-13, 16-19, 23-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cypher (U.S. Patent application number 2004/0088636).

10. As per claim 3, Cypher does not explicitly disclose insuring write access is not prohibited. Cypher teaches as stated per claim 1 above a data remap control circuit is configured to cause a remap of each of a plurality of encoded data blocks to avoid storing bits in the failing memory device. He thus teaches disabling access to the failed memory module. He also teaches (Page 3, para. 0039, lines 8-11) that correction may include reconstructing the data that was stored in the failed memory device using the check bits. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to realize that He also ensures that write access is not prohibited, since he teaches that correction may include reconstructing the data that was stored in the failed memory device using the check bits, therefore would not prohibited write access.

11. As per claim 4, With reference to logging information regarding the error and determining the error type based at least on the error. He teaches (Page 3, para. 0040, lines 1-5) that the persistent state storage 20 is configured to record state information regarding the persistent failures, which have been detected by the memory controller.

12. As per claim 5, With reference to reconstructing data that caused the failed memory module to fail and servicing a memory request with the reconstructed data. He teaches (Page 3, para. 0039, lines 8-11) that correction may include reconstructing the data that was stored in the failed memory device using the check bits.

13. As per claim 6, With reference to scrubbing the failed memory module with the reconstructed data. He teaches (Page 3, para. 0039, lines 8-11) that correction may include

reconstructing the data that was stored in the failed memory device using the check bits. He thus performs scrubbing the failed memory module with the reconstructed data.

14. As per claim 7, With reference to the determining the error type based on the error and prior errors. He teaches (Page 3, para. 0039, lines 28-33).

15. As per claim 8, With reference to the error type is determined based on an error threshold. He teaches (Page 3, para. 0040, lines 7-9).

16. As per claim 9, With reference to enabling access to the failed memory module when an error threshold is not exceeded. He teaches (Page 3, para. 0039, lines 36-38).

17. As per claim 10, With reference to disabling access to the failed memory module when an error threshold is exceeded. He teaches (Page 3, para. 0039, lines 16-18).

18. As per claims 11 & 12, With reference to the error threshold comprises an error rate. He teaches (Page 3, para. 0040, lines 7-9).

19. As per claim 13, With reference to continuing access to the failed memory module based on the error type. He teaches (Page 3, para. 0039, lines 7-9). With reference to continuing to disable read access to the failed memory module when the error type is determined to be hard and enabling read access to the failed memory module when the error type is determined to be soft. He teaches (Page 3, para. 0039, lines 11-14).

20. As per claim 16, He does not explicitly disclose a memory module access configurator that configures access the redundant memory controller has to the failed data storage device based on the type of memory error. He also teaches data remap control circuit is configured to cause a remap of each of a plurality of encoded data blocks to avoid storing bits in the failing

memory device. He thus teaches configuring access to the memory module based on the error type.

21. As per claim 17, With reference to the error type is determined based on an error threshold. He teaches (Page 3, para. 0040, lines 7-9).

22. As per claims 18 & 19, With reference to the error threshold comprises an error rate. He teaches (Page 3, para. 0040, lines 7-9).

23. As per claims 23 & 24, He teaches (Page 3, para. 0040, lines 1-5) that the persistent state storage 20 is configured to record state information regarding the persistent failures, which have been detected by the memory controller.

24. As per claims 25 & 26, With reference to the error type is determined based on an error threshold. He teaches (Page 3, para. 0040, lines 7-9).

25. As per claims 27 & 28, With reference to the error threshold comprises an error rate. He teaches (Page 3, para. 0040, lines 7-9).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nadeem Iqbal whose telephone number is (571)-272-3659. The examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)-272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nadeem Iqbal
Primary Examiner
Art Unit 2114

NI